

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		10595384	
	Filing Date		2006-04-13	
	First Named Inventor	Christopher Hess		
	Art Unit	2857		
	Examiner Name			
Attorney Docket Number		D5116-00051		

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	1	6449749		2002-09-10	Stine	
	2	7024642		2006-04-04	Hess et al.	

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	1	20060101355		2006-05-11	Dennis Ciplickas et al.	

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
	1	Stapper, C. H., Rosner, R. J., "Integrated Circuit Yield Management and Yield Analysis: Development and Implementation," IEEE Transactions on Semiconductor Manufacturing, pp. 95-102, Vol. 8, No. 2, 1995	<input type="checkbox"/>
	2	Iprì, A. C., Sarace, J. C., "Integrated Circuit Process and Design Rule Evaluation Techniques," RCA Review, pp. 323-350, Volume 38, Number 3, September 1977	<input type="checkbox"/>
	3	Buehler, M. G., "Microelectronic Test Chips for VLSI Electronics," VLSI Electronics Microstructure Science, pp. 529-576, Vol. 6, Chapter 9, Academic Press, 1983	<input type="checkbox"/>
	4	Doong, K., Cheng, J., Hsu, C., "Design and Simulation of Addressable Failure Site Test Structure for IC Process Control Monitor," pp. 219-222, International Symposium on Semiconductor Manufacturing, 1999	<input type="checkbox"/>
	5	Hess, C., Weiland, L. H., "Influence of Short Circuits on Data of Contact & Via Open Circuits Determined by a Novel Weave Test Structure," IEEE Transactions on Semiconductor Manufacturing, pp. 27-34, Vol. 9, No. 1, 1996	<input type="checkbox"/>
	6	Hess, C., Stashower, D., Stine, B. E., Weiland, L. H., Verma, G., Miyamoto, K., Inoue, K., "Fast Extraction of Defect Size Distribution Using a Single Layer Short Flow NEST Structure", IEEE Transactions on Semiconductor Manufacturing, pp. 330-337, Vol. 14, No. 4, 2001	<input type="checkbox"/>
	7	Wallon, A. J., Ward, D., Robertson, J. M., Holwill R. J., "A Novel Approach for an Electrical Vernier to Measure Mask Misalignment", pp. 950-953, 19th European Solid State Device Research Conference ESSDERC '89, Springer Verlag, 1989	<input type="checkbox"/>
	8	Hess, C., Stine, B. E., Weiland, L. H., Mitchell, T., Karnett, M., Gardner, K., "Passive Multiplexer Test Structure For Fast and Accurate Contact and Via Fail Rate Evaluation", pp. 163-167, Proc. International Conference on Microelectronic Test Structures (ICMTS), Vol. 15, Cork (Ireland), 2002	<input type="checkbox"/>
	9	Wallon, A. J., Gammie, W., Marrow, D., Stevenson, J. T. M., Holwill, R. J., "A Novel Approach for Reducing the Area Occupied by Contact Pads on Process Control Chips", International Conference on Microelectronic Test Structures, San Diego, (USA), 1990	<input type="checkbox"/>
	10	Hess, C., Weiland, L. H., Bornfeld, R., "Customized Checkerboard Test Structures to Localize Interconnection Point Defects", Proc. VLSI Multilevel Interconnection Conference (VMIC), pp. 163-168, Santa Clara (USA), 1997	<input type="checkbox"/>

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11	Hess, C., Weiland, L. H., "Defect Parameter Extraction in Backend Process Steps using a Multilayer Checkerboard Test Structure", Proc. International Conference on Microelectronic Test Structures (ICMTS), pp. 51-56, Nara (Japan), 1995	<input type="checkbox"/>
12	Hess, C., Weiland, L. H., "Strategy to Disentangle Multiple Faults to Identify Random Defects within Test Structures", Proc. International Conference on Microelectronic Test Structures (ICMTS), pp. 141-146, Kanazawa (Japan), 1998	<input type="checkbox"/>
13	Hess, C., Weiland, L. H., "Harp Test Structure to Electrically Determine Size Distributions of Killer Defects", IEEE Transactions on Semiconductor Manufacturing, pp. 194-203, Vol. 11, No. 2, 1998	<input type="checkbox"/>
14	Hess, C., Weiland, L. H., "Drop in Process Control Checkerboard Test Structure for Efficient Online Process Characterization and Defect Problem Debugging", Proc. International Conference on Microelectronic Test Structures (ICMTS), pp. 152-159, San Diego (USA), 1994	<input type="checkbox"/>
15	Hess, C., Weiland, L. H., Lau, G., Simoneit, P., "Control of Application Specific Interconnection on Gate Arrays Using an Active Checkerboard Test Structure", Proc. International Conference on Microelectronic Test Structures (ICMTS), pp. 55-60, Trento (Italy), 1996	<input type="checkbox"/>
16	Doong, K., Hsieh, S., Lin, S., Shen, B. Cheng, J., Hess, C., Weiland, L., Hsu, C., "Addressable Failure Site Test Structures (AFS-TS) for CMOS Processes: Design Guidelines, Fault Simulation, and Implementation", IEEE Transactions on Semiconductor Manufacturing, pp. 338-355, Vol. 14, No. 4, 2001	<input type="checkbox"/>
17	Ward, D., Walton, A. J., Gammie, W. G., Holwill, R. J., "The Use of a Digital Multiplexer to Reduce Process Control Chip Pad Count", International Conference on Microelectronic Test Structures, Vol. 5, San Diego (USA), 1992	<input type="checkbox"/>
18	Khare, J., Maly, W., Griep, S., Schmitt-Landsiedel, D., "SRAM-based Extraction of Defect Characteristics", International Conference on Microelectronic Test Structures, Vol. 7, San Diego, USA, 1994	<input type="checkbox"/>

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Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

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☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

- ☐ See attached certification statement.
- ☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.
- ☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.16. Please see CFR 1.4(d) for the form of the signature.

Signature	/Richard A. Paikoff/	Date (YYYY-MM-DD)	2007-08-15
Name/Print	Richard A. Paikoff	Registration Number	34,892

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